Eighth Quarterly Report

for

PHOTON-COUPLED ISOLATION SWITCH

(1 October to 31 December 1967)

Contract No. 951340

Prepared by

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Jet Propulsion Laboratory
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ABSTRACT

A new type of integrated circuit switch which uses internal photon generation and detection techniques is being developed. Internal optical coupling is used to allow electrical isolation between the driving source and the output switch terminals. The device, called the photon-coupled isolation switch, consists of a monolithic silicon integrated driver circuit which supplies bias to a gallium arsenide (GaAs) photon-emitting diode. The emitting diode is optically coupled to an electrically-isolated silicon (Si) phototransistor which provides the isolated output switch terminals.

The development program for this three-wafer integrated circuit consists of two phases:

- Phase I, design and breadboarding of the driver circuit and development of the emitting diode–phototransistor pair (GaAs switch).
- Phase II, integration of the driver circuit and prototype production of the complete isolation switch.

Phase I was previously completed with an evaluation of the driver circuit breadboard and development of the GaAs switch. Under Phase II, integrated circuit masks for processing the monolithic driver circuits were designed and fabricated. The processing was begun and some marginal driver circuits were produced.

During the last quarter of the program, the integrated circuit processing was continued. Good driver circuit wafers were produced. Isolation switches were assembled, tested and found to satisfy the design requirements and device specifications.

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SECTION I
INTRODUCTION

The function of an isolation transformer provides the system designer with the capability of coupling signals between circuits operating at different dc potentials. The absence of common ground connections also produces signal coupling without the introduction of interference from extraneous ground noise. Unfortunately, the isolation function cannot be effectively provided with the processing techniques used in conventional integrated circuits. However, in the present contract, a new type of integrated circuit isolation switch is under development, using optoelectronic techniques. This device will use internal photon generation and detection to provide output switch terminals which are electrically isolated from all other terminals of the switch. Efficient signal coupling is being obtained using a gallium arsenide (GaAs) P-N junction, photon-emitting diode coupled with a silicon (Si) P-N junction photodetector, both of which have photo responses which peak near 0.9 μm at 25°C. Previously developed isolation devices which use the GaAs-Si optical pair include an isolated-input transistor, an isolated-gate PNPN-type switch, a multiplex switch requiring no driving transformer, and an isolated-input pulse amplifier.[1,2,3]

The isolation switch under development in the present contract combines three semiconductor wafers:

A monolithic Si integrated circuit,

A GaAs photon-emitting diode, and

A Si phototransistor.

The integrated circuit wafer consists of a ten-input DTL gate that is designed to supply forward current to the GaAs diode, biasing it into the photon-emission mode. Photons are coupled from the emitting diode to the phototransistor through a layer of high-refractive-index glass. This minimizes losses at material interfaces that, in the case of an air coupling medium, could result due to the high refractive indices of GaAs and Si. Photon absorption near the collector-base PN junction biases the transistor as would electrical biasing.

The development program is divided into two phases. Phase I was completed[4] with the development of the emitting diode–phototransistor pair (GaAs switch) and the design and breadboarding of the driver circuit. Under Phase II, the Si monolithic circuit (driver circuit) is to be produced and the three-wafer isolation switch is to be assembled in an integrated circuit flat package. Previously, under Phase II, the integrated circuit component layout was developed and processing was initiated. This report describes activities carried out during the previous quarter of the program, that resulted in the production of good driver circuit wafers; subsequently, complete isolation switches were assembled which met the design requirements and device specifications.

SECTION II
TECHNICAL DISCUSSION

A. ISOLATION SWITCH TESTING

1. Fabrication Process Evaluation

The detailed assembly steps for the isolation switch were previously described.[5] Preliminary evaluation of this processing was conducted with isolation switches built using electrically inferior semiconductor wafers. The most important result of this procedure was a change in the choice of the integrated circuit flat package. The first type of package was selected for its large glass-free wafer mounting area. There was also a region in the center of the bottom where gold plating was missing. Because this package is usually used with silicon chips mounted with glass frit, the gold-free area is usually unimportant. For the isolation switch, however, metallized ceramic wafers are mounted to the package bottom using alloy preforms. In the first package, the alloy tended to flow to the plated portion of the package bottom, resulting in lumps of excess alloy around the bottom of the ceramic wafers. The new package is dimensionally identical to the former package, but the bottom is completely plated. Isolation switches mounted in the new packages show no gold lups.

No significant problems developed in wafer mounting or lead bonding, which verified that the assembly procedure was adequate.

2. Electrical Evaluation

Preliminary electrical evaluation was performed on five isolation switches built with good semiconductor wafers. Circuit parameters, measured at -20° C, 25° C, and 100° C, are given in Tables I and II, along with the design specifications and measurement conditions. The test procedure used is described in the Appendix. The ten input diode terminals were connected together to give worst-case values of the power dissipation in the OFF-condition, P_{OFF}, the input diode current in the ON- and OFF-conditions, and the input diode breakdown voltage. For these tests, the diode breakdown was determined as the difference between the input voltage and the supply voltage, less 0.2 V for the drop across the resistor in series with the input diodes and the power supply, R_1.

The data show that only one isolation switch met all design specifications. Four devices failed to satisfy the specification for the phototransistor current, I_C at V_{CE} = 0.6 V, V_{CC} = 3.5 V, and T = 100 C, and one of these also had an excessive turn-ON time, t_1, at V_{CC} = 3.5 V. These parameters are related to the light emission of the GaAs diode, the optical coupling and phototransistor gain. As indicated by the satisfactory performance of Phase I GaAs switches,[4] these results are not typical of that expected for the isolation switches. Selection techniques used for the GaAs diodes and phototransistors insure sufficient optical coupling to meet the specifications for I_C and t_1.

Table I. Preliminary Isolation Switch Characteristics

Parameter	Specification		Device					Conditions				
	Value	Unit	1	2	3	4	5	T (°C)	V_{CC} (V)	V_{In} (V)	V_{CE} (V)	I_C (mA)
P_{ON}	⩽200	mW	164	160	165	158	166	25	4.5	6	–	–
P_{ON}	⩽200	mW	171	170	172	167	171	-20	4.5	6	–	–
P_{ON}	⩽200	mW	144	143	145	139	142	100	4.5	6	–	–
P_{OFF}	⩽1	mW	0.86	0.90	0.90	0.90	0.90	25	4.5	0	–	–
P_{OFF}	⩽1	mW	0.86	0.90	0.90	0.90	0.91	-20	4.5	0	–	–
P_{OFF}	⩽1	mW	0.81	0.83	0.83	0.86	0.84	100	4.5	0	–	–
I_I	$\leqslant 5 \times 10^4$	nA	≪1	≪1	≪1	≪1	≪1	25	4.5	6	–	–
I_I	$\leqslant 5 \times 10^4$	nA	≪1	≪1	≪1	≪1	≪1	-20	4.5	6	–	–
I_I	$\leqslant 5 \times 10^4$	nA	24.8	28.0	23.0	42.0	36.0	100	4.5	6	–	–
I_I	⩽-1	mA	-0.189	-0.197	-0.197	-0.195	-0.198	25	4.5	0	–	–
I_I	⩽-1	mA	-0.190	-0.200	-0.200	-0.200	-0.200	-20	4.5	0	–	–
I_I	⩽-1	mA	-0.174	-0.178	-0.179	-0.178	-0.180	100	4.5	0	–	–
BV_{DI}	⩾6.5	V	7.9	8.0	7.9	8.0	7.9	25	–	–	–	–
BV_{CEO}	⩾35	V	72	84	75	70	86	25	–	–	–	1
I_{CEO}	⩽100	nA	1	1.3	1	1.2	1.1	25	–	–	20	–

Additional tests of the isolation switch were made at 25° C, using a breadboard connection of various driver circuit wafers and a representative GaAs photon emitting diode. The data for six units, shown in Table III, consist of:

- The emitting diode current, I_{D2}, for a worst-case ON-condition (with the supply voltage V_{CC} = 3.5 V and the input voltage V_{IN} = 6 V) and OFF-condition (with V_{CC} = 4.5 V and V_{IN} = 1 V)
- The power dissipation, P_{ON}, in a worst-case ON-condition (with V_{CC} = 4.5 V and V_{IN} = 6 V)
- The breakdown voltage of the input diode, BV_{D1},
- The input diode current, I_{IN}, in a worst-case ON-condition (with V_{CC} = 4.5 V and V_{IN} = 0).

Values obtained for P_{ON}, BV_{D1}, and I_{IN} agree closely with those in Table I. From the worst-case design[6], the calculated minimum value for I_{D2} at 25 C in the ON-condition, $I_{D2(ON)}$, is 24.0 mA. In Table III, five devices have values of $I_{D2(ON)}$ between 24.3 and 24.6 mA. For one device, $I_{D2(ON)}$ was 23.8 mA, which is within the measuring accuracy of the worst-case value. Values in Table III for I_{D2} in the OFF-condition, $I_{D2(OFF)}$, range from 43 to 48 nA; this current level results in negligible photo emission and, thereby, photo-induced leakage in the phototransistor.

Table II. Preliminary Isolation Switch Output Characteristics

Parameter	Specification		Device					Conditions				
								T	V_{CC}	V_I	V_{CE}	I_C
	Value	Unit	1	2	3	4	5	(°C)	(V)	(V)	(V)	(mA)
I_{CEO}	100	nA	1.4	1.9	1.4	1.8	1.3	25	4.5	1	20	–
I_{CEO}	100	nA	<1	<1	<1	<1	<1	-20	4.5	1	20	–
I_{CEO}	10	μA	5.95	4.8	6.3	9.4	3.0	100	4.5	1	20	–
V_{CES}	0.6	V	0.14	0.17	0.14	0.17	0.17	+25	3.5	3	–	10
V_{CES}	0.6	V	0.14	0.14	0.11	0.14	0.14	-20	3.5	3	–	10
V_{CES}	0.6	V	0.36	0.31	0.23	0.31	0.38	100	3.5	3	–	10
V_{CES}	0.6	V	0.4	0.26	0.24	0.30	0.27	25	3.5	3	–	15
V_{CES}	0.6	V	0.22	0.20	0.15	0.23	0.23	-20	3.5	3	–	15
V_{CES}	0.6	V	–	–	0.39	–	–	100	3.5	3	–	15
I_C	15	mA	18.5	19.2	27.5	18.5	19.2	25	3.5	3	0.6	–
I_C	15	mA	23.0	17.0	31.0	18.2	18.6	-20	3.5	3	0.6	–
I_C	15	mA	12.5	13.2	18.5	13.4	12.5	100	3.5	3	0.6	–

Switching Times										V_I = Pulse (V)	V_{CE} (V)	I_C (MA)
										Pulse	OFF	ON
t_1	10	μs	10	7.4	6.3	11.6	7.4	25	3.5	3	20	10
t_1	10	μs	6	4.6	4.0	6.6	4.2	25	4.5	3	20	10
t_2	100	μs	40	24	42	41	23	25	3.5	3	20	10
t_2	100	μs	43	27	43	45	25	25	4.5	3	20	10

Table III. Characteristics of Several Isolation Switches

Device	$I_{D2(ON)}$ (mA) V_{CC} = 3.5 V V_{IN} = 6 V	$I_{D2(OFF)}$ (nA) V_{CC} = 4.5 V V_{IN} = 1 V	P_{ON} (mW) V_{CC} = 4.5 V V_{IN} = 6 V	BV_{D1} (V) I_{IN} = 10 A	I_{IN} (mA) V_{CC} = 4.5 V V_{IN} = 0
1	23.8	48	160	8.3	-0.192
2	24.3	43	167	8.2	-0.196
3	24.4	44	164	8.2	-0.190
4	24.8	43	166	8.2	-0.198
5	24.3	45	162	8.2	-0.192
6	24.6	43	164	8.2	-0.196

A primary relationship in the design of the driver circuit for the OFF-condition is that between the input voltage and the voltage applied to the emitting diode. A detailed measurement was made of this characteristic for a representative driver circuit and emitting diode. The results are described in Figure 1. The relationship between input voltage and emitting diode current for the same devices is shown in Figure 2. These results are within the design tolerances.

3. Environmental Test Evaluations

The isolation switches that were mounted in the new package for evaluation of the device assembly techniques were continued through final processing. Preliminary environmental tests were

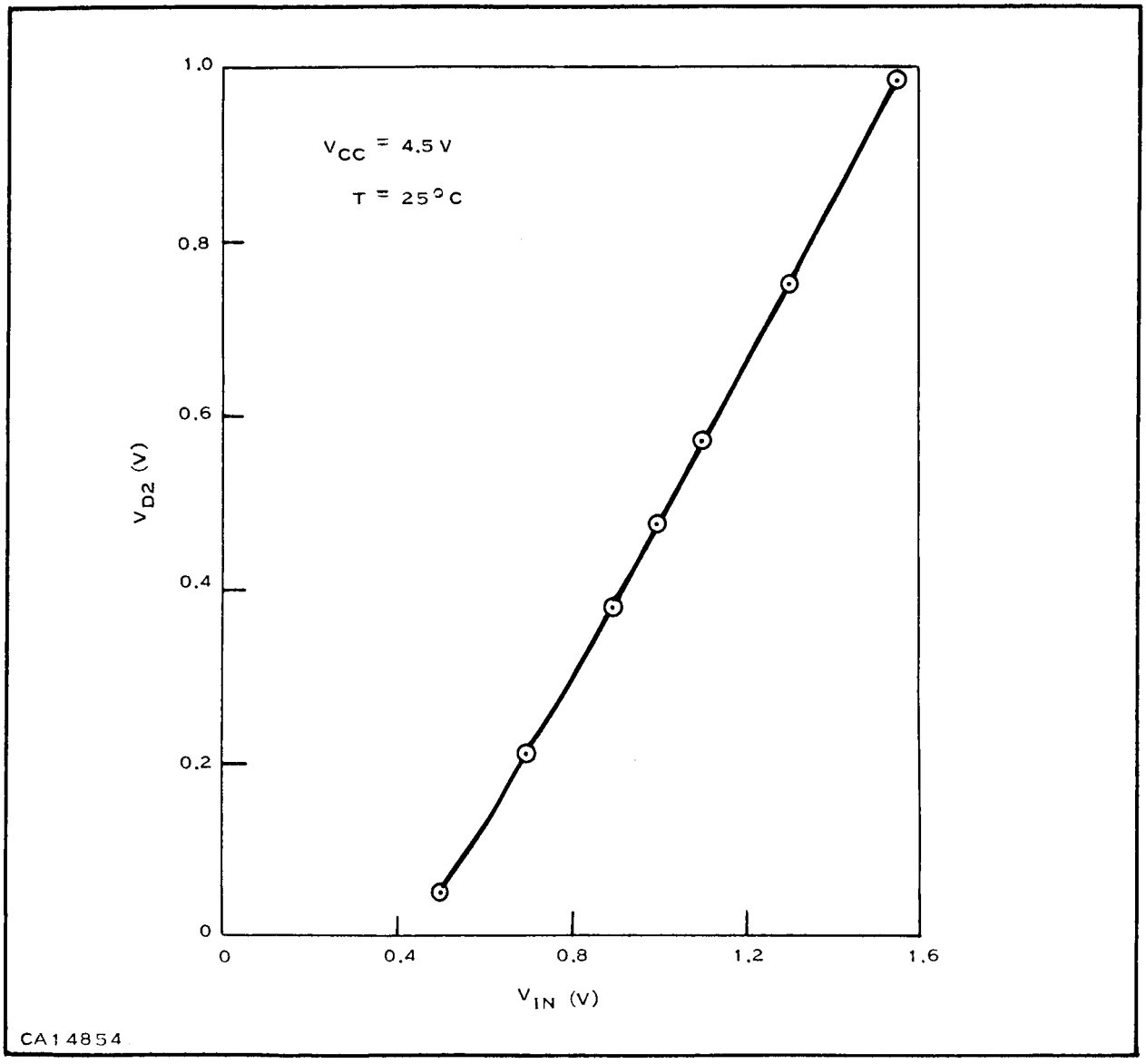

Figure 1. Input Voltage–Emitting Diode Voltage Characteristic for Representative Isolation Switch

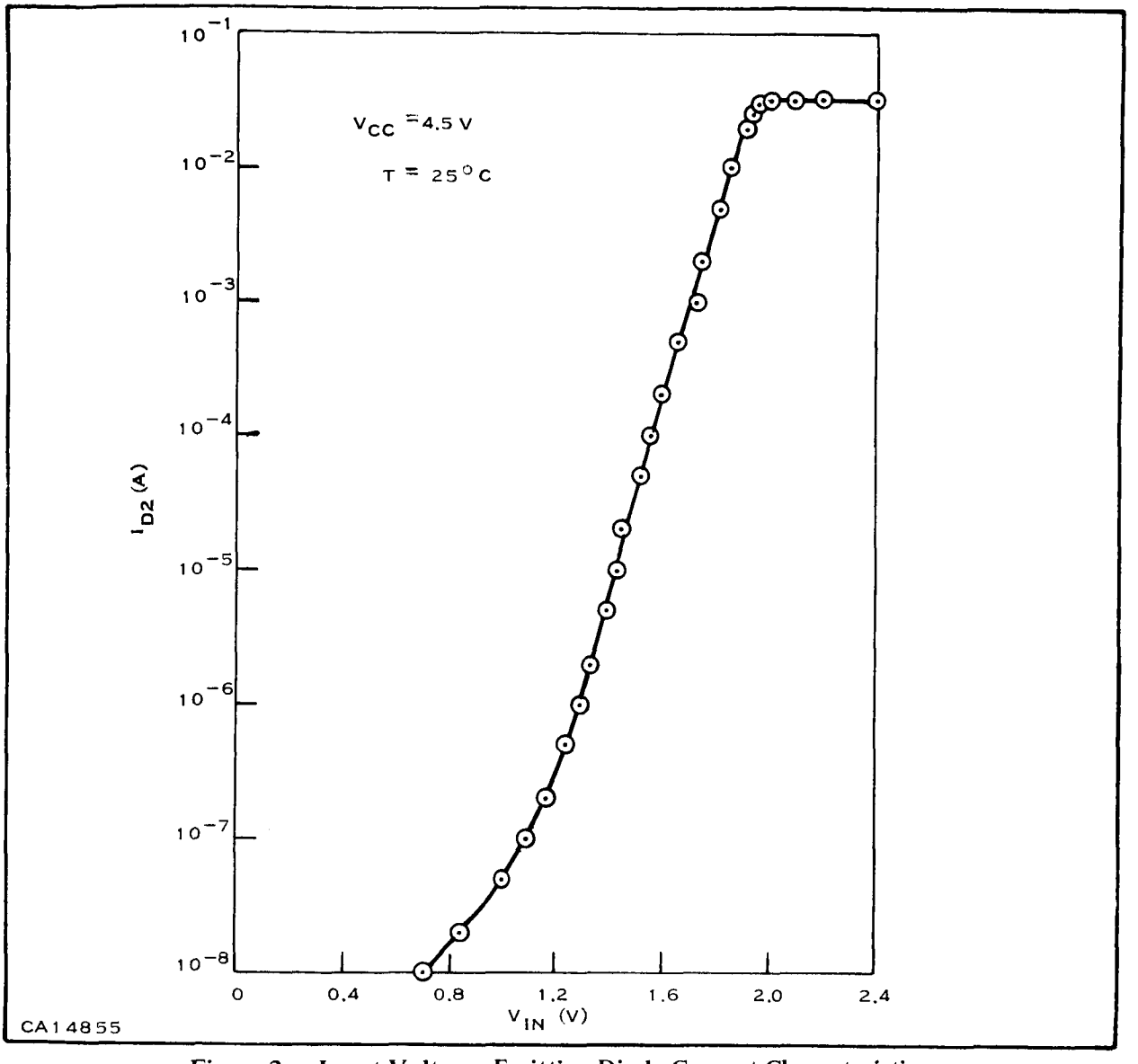

Figure 2. Input Voltage–Emitting Diode Current Characteristic for Representative Isolation Switch

conducted to examine the units for gross defects. A process lot of 16 units was separated into three groups, submitted for environmental testing, and tested electrically for open or short-circuited leads and for isolation of chips from each other and the package. The tests performed were:

- Variable Frequency Vibration—20 to 2000 to 20 Hz at 50 g, three perpendicular planes, 15 minutes per plane.
- Mechanical Shock—10,000 g, 0.2 ms onset time, all six planes, five blows per plane.
- Temperature Cycling—10 cycles consisting of 15 minutes at -65° C, 5 minutes at 25° C, 15 minutes at 150° C, and 5 minutes at 25° C.

No failures were noted. These tests support the recommendation based on tests with GaAs switches made earlier[6] that temperature cycling should be limited to -65° C and 150° C.

Following these tests, four electrically good isolation switches (Nos. 1, 2, 4, and 5 described in Table I) were subjected to the previously described environmental tests and to acceleration of 20,000 g's for a period of one minute, with the units mounted in each of three mutually perpendicular planes. The evaluation tests consisted of operational measurements and tests for isolation. None of the devices exhibited lead or bond fracture, or change in the isolation or the optical coupling.

B. DEVICE STUDIES

Recently processed phototransistors have exhibited somewhat greater collector-to-emitter leakage currents, I_{CEO}, at higher temperatures. A significant characteristic is the relation between I_{CEO} at 25° C and at 100°C, as illustrated in Figure 3. The leakage current at 100° C is now greater for devices having the same value of 25°C leakage. As a result, the yields have been low. Two possible causes are:

- The current gain at low-current levels is now relatively greater at 100°C.
- The leakage current, I_{CBO}, is now greater and the current gain at low currents is now relatively lower at 25°C.

Transistor processing is being evaluated to determine if some apparently subtle change that affected the leakage current change can be identified. This procedure of slightly modifying the process to compensate for various "minor" process variations and uncontrolled effects is well established in the art of transistor production. The studies underway should promptly result in lowering of the leakage current levels at 100° C.

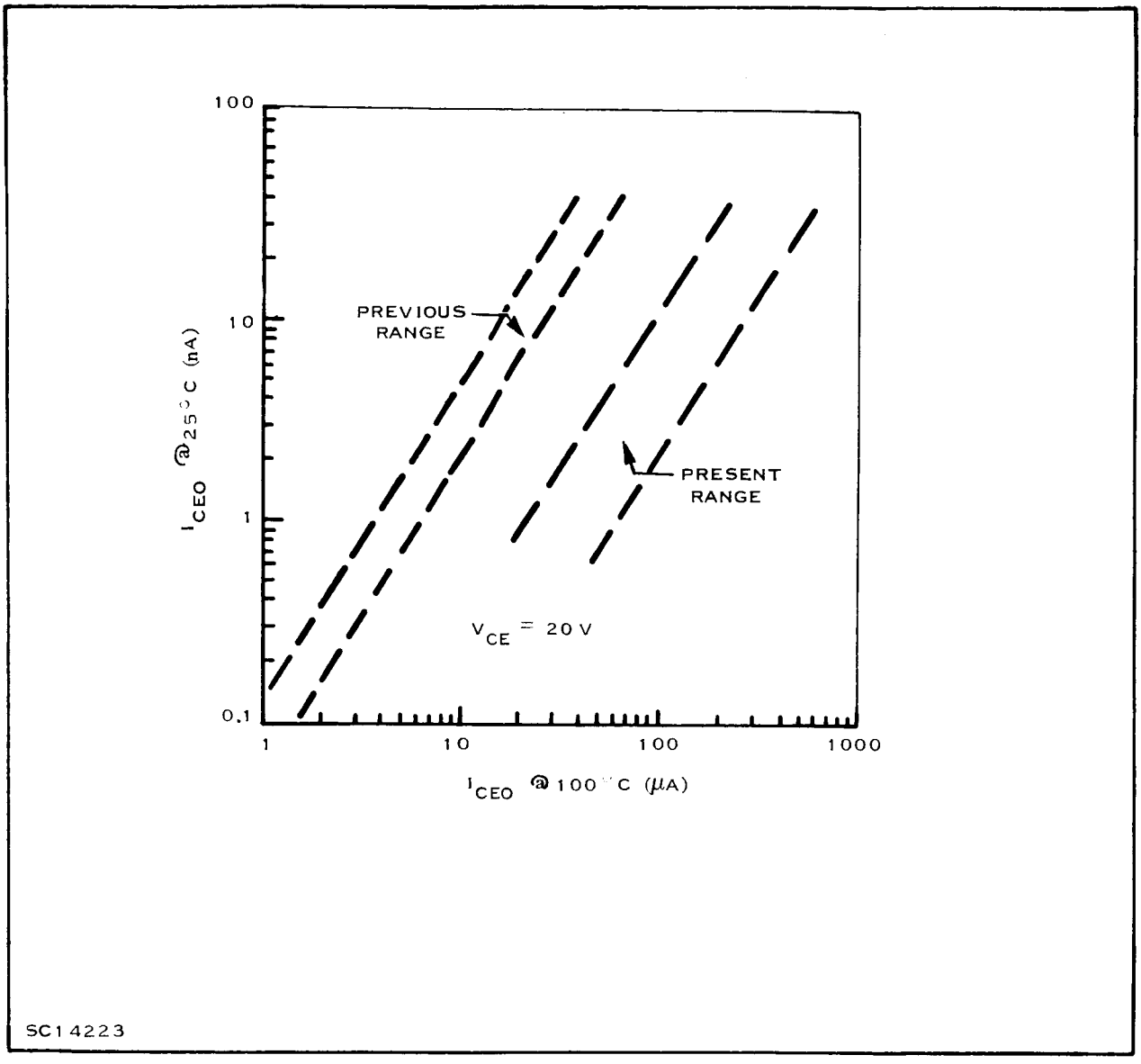

Figure 3. Phototransistor Collector-Emitter Leakage Current Characteristic

SECTION III
CONCLUSIONS AND RECOMMENDATIONS

Good integrated driver circuits were produced. Complete isolation switches were fabricated which satisfy the device specifications.[5] Production of the isolation switches will be directed toward fabrication of the deliverable devices.

SECTION IV
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4. E. L. Bonin, "Photon Coupled Isolation Switch," Texas Instruments Incorporated, JPL Contract No. 951340, Fifth Quarterly Report, 1 January to 31 March, 1967.

5. E. L. Bonin and E. E. Harp, "Photon Coupled Isolation Switch," Texas Instruments Incorporated, JPL Contract No. 951340, Seventh Quarterly Report, 1 July to 30 September, 1967.

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APPENDIX

ISOLATION SWITCH TEST PROCEDURE

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ISOLATION SWITCH TEST PROCEDURE

This test procedure defines device and test parameters and describes test conditions for the complete isolation switch. A functional representation of the isolation switch, with the terminal parameters defined, is shown in Figure A-1. Components of the driver circuits are identified in the isolation switch schematic, Figure A-2. Parameter design specifications and measurement conditions are described in Table A-1. Other conditions may be used in the report for device evaluation purposes. The test circuits for measuring switching times and noise transmissibility are shown in Figures A-3 and A-4, respectively. The power supply's voltage design range is 3.5 to 4.5 V, and the ambient temperature range is -20 to 100°C.

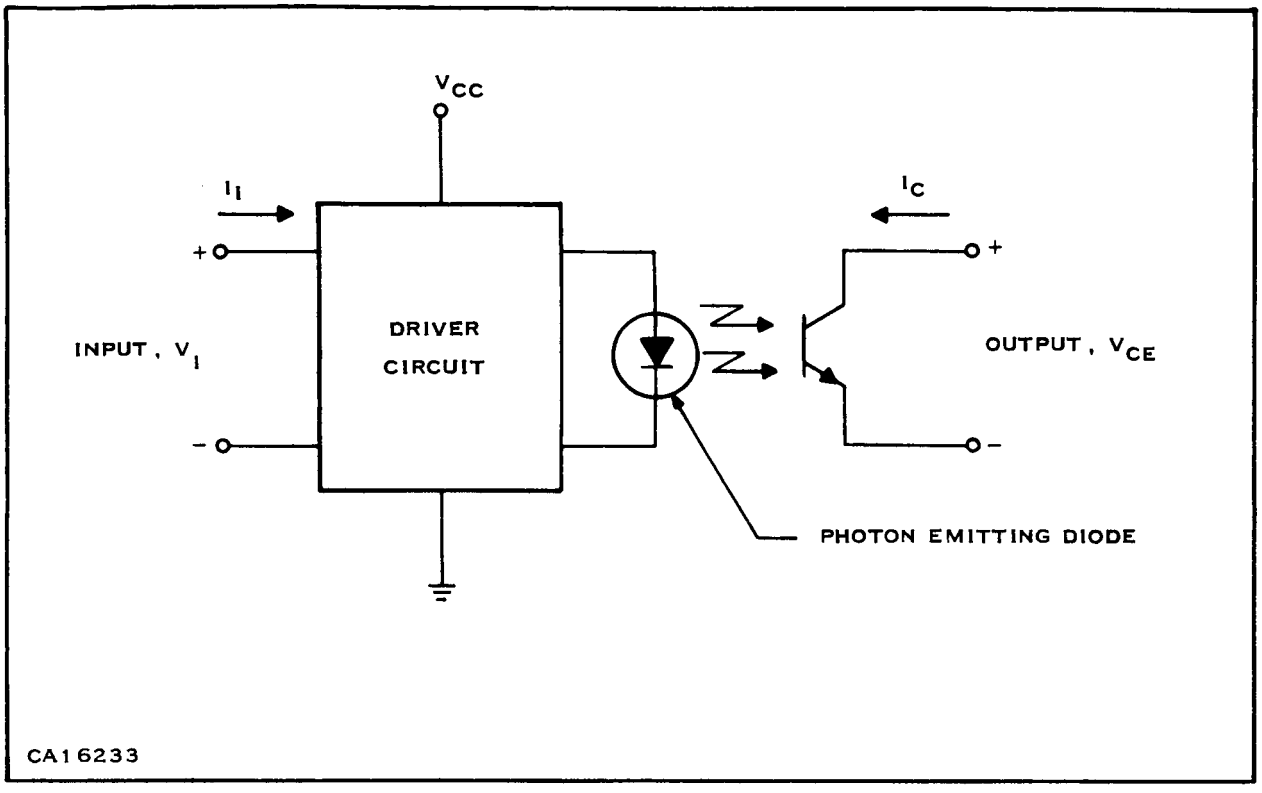

Figure A-1. Photon Coupled Isolation Switch

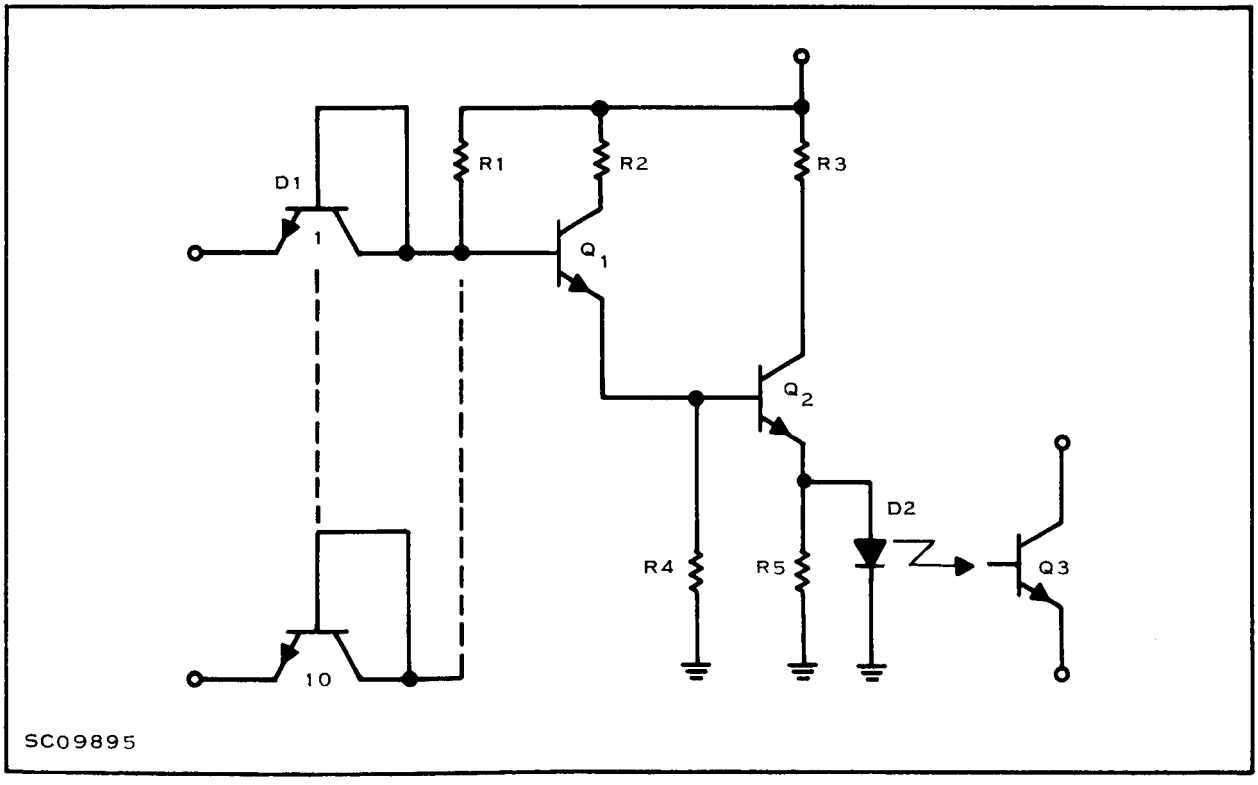

Figure A-2. Isolation Switch Schematic

Table A-I. Isolation Switch Specifications

Parameter	Symbol	Conditions	Value Min	Value Max	Unit
Input Voltage:					
at "1" level	V_I		3.0	6.0	V
at "0" level	V_I		0	1.0	V
Input Current:					
at "1" level	I_I	V_I = 6 V		50	μA
at "0" level	I_I	V_I = 0.1 V		-1.0	mA
Output Saturation (ON) Voltage	V_{CES}	V_I = 3 V, I_C = 10 mA		0.6	V
Output (ON) Current	I_C	V_I = 3 V, V_{CES} = 0.6 V	10		mA
Output Leakage (OFF) Current	I_{CEO}	V_I = 1 V, V_{CE} = 20 V			
		Temp. = +25°C		0.1	μA
		Temp. = +100°C		20	μA
Output Breakdown Voltage	BV_{CEO}	V_I = 0 V, I_C = 100 μA	35		V
Isolation Capacitance (between output and all other terminals)	C_{ISO}	freq = 1.0 kHz		10	pF
Switching Times:					
Turn ON	t_1	(See Figure A-3)		10	μs
Turn OFF	t_2	(See Figure A-3)	100	μs	
Noise Transmissibility	V_n	(See Figure A-4)		2.0	V
Power Dissipation:					
Switch ON	P_{ON}	V_I = 3 V, I_C = 0		200	mW
Switch OFF	P_{OFF}	V_I = 0 V, I_C = 0		1.0	mW

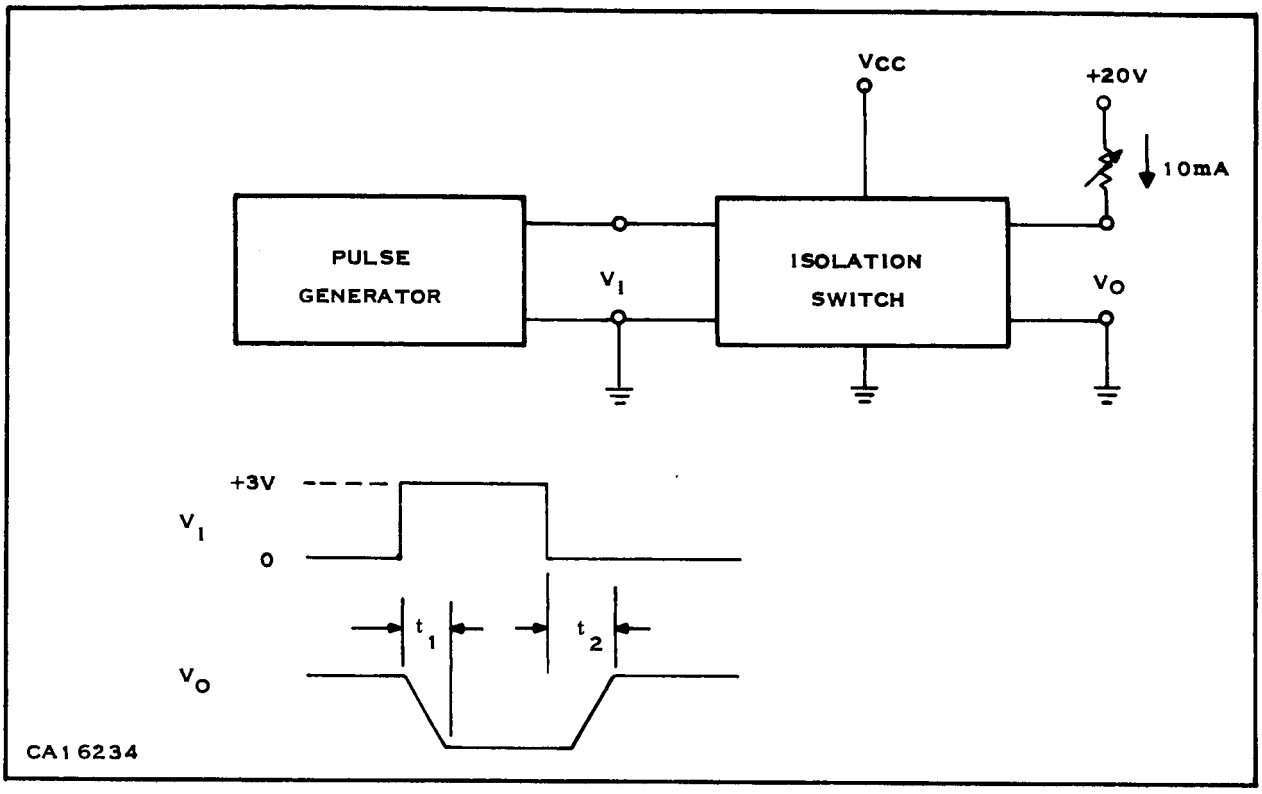

Figure A-3. Switching Time Test

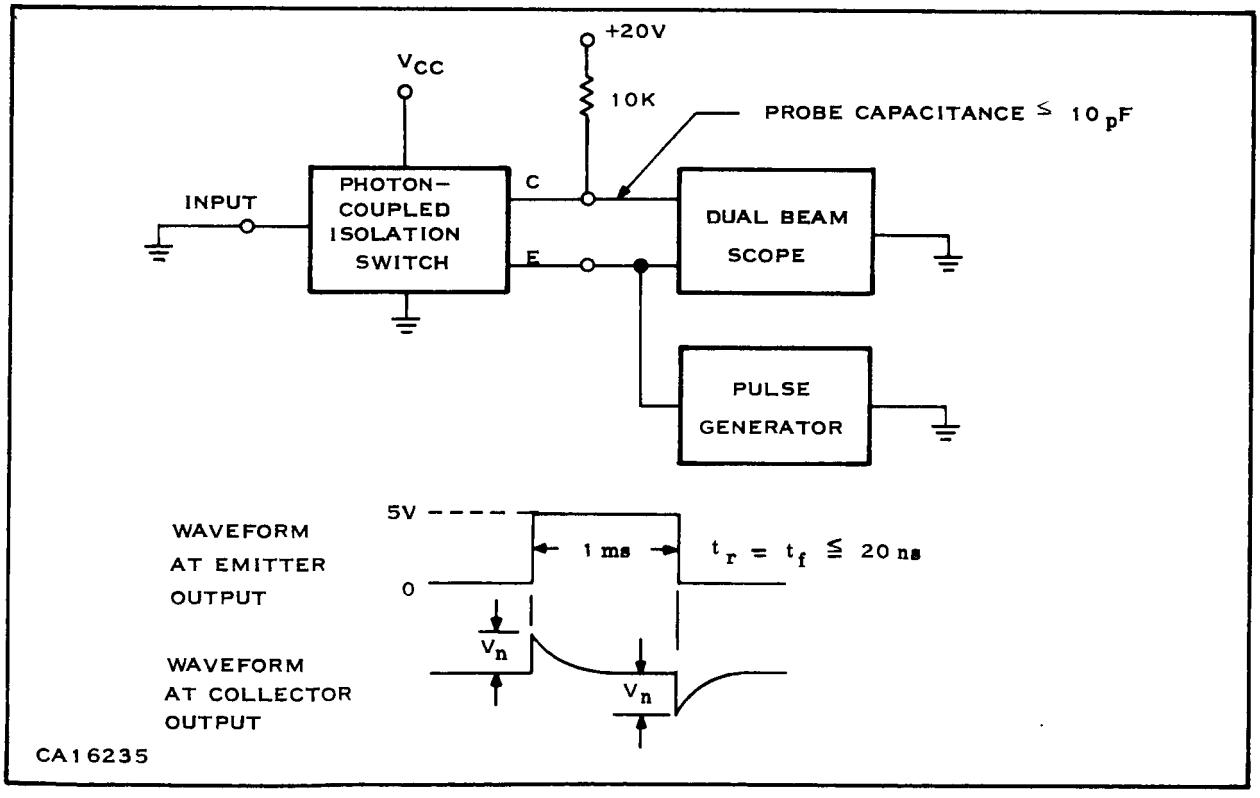

Figure A-4. Noise Transmissibility Test